CLAIMS

What is claimed is:

1. A base station controller for a wireless network, comprising:

a plurality of processor boards, each processor board comprising a local timer; and

a timing unit for generating timing cells, each timing cell containing time information, the timing unit transmitting timing cells to the respective processor boards,

wherein a processor board realigns its local timer with time information contained in a received timing cell whenever its local timer drifts from the time information contained in the timing cell outside of a predetermined time window.

2. The base station controller of claim 1, wherein the predetermined time window is approximately 2 ms.

3. The base station controller of claim 1, wherein the timing cells are transmitted to the processor boards over an Asynchronous Transfer Mode (ATM) network.

4. The base station controller of claim 1, wherein the timing cells are transmitted to the processor boards over an Ethernet network.

5. The base station controller of claim 1, wherein the timing cells are transmitted to the processor boards over a universal serial bus.

6. The base station controller of claim 1, wherein the time information contained in the respective timing cells is generated based on both a universal coordinated time received from a GPS receiver, and a reference clock received from a PSTN.

7. The base station controller of claim 6, wherein the reference clock has a frequency of 8 KHz.

8. The base station controller of claim 6, wherein the timing unit comprises

means for multiplying the frequency of the reference clock;

a counter receiving the frequency multiplied reference clock and a GPS event signal from the GPS receiver, wherein the counter free-runs off the frequency multiplied reference clock, reloads when it receives the GPS event signal, outputs a count value, and outputs an interrupt signal when it rolls over; and

a device board module receiving the count value and the interrupt signal from the counter and receiving the universal coordinated time from the GPS receiver, wherein the device board module keeps track of time based on the received universal coordinated time and the received count value, and the device board module generates and transmits at least one timing cell when it receives the interrupt signal from the counter.

9. The base station controller of claim 8, wherein the counter receives the GPS event signal from the GPS receiver at a frequency of 1 Hz.

10. The base station controller of claim 1, wherein at least one of the processor boards is a media stream board for receiving speech samples from pulse code modulated speech signals and for compressing the received speech samples into frames of compressed speech data.

11. The base station controller of claim 10, wherein the media stream board drops or repeats a portion of the received speech samples when the media stream board realigns its local timer with the time contained in a received timing cell.

12. The base station controller of claim 11, wherein the predetermined time window of the media stream board is approximately 2 ms.

13. The base station controller of claim 10, wherein the media stream board compresses groups of 160 of the received speech samples into 20 ms vocoded frames of compressed speech data.

14. The base station controller of claim 13, wherein the media stream board drops about 1 ms worth of the received speech samples when the media stream board realigns its local timer with the time contained in a received timing cell.

15. The base station controller of claim 13, wherein the media stream board repeats a vocoded frame when the media stream board realigns its local timer with the time contained in a received timing cell.

16. In a wireless network, a base station controller comprising a plurality of processor boards, each processor board having a local timer, a method for reducing the occurrence of audible noise in the base station controller, comprising:

generating a plurality of timing cells, each timing cell containing time information;

transmitting the timing cells to the processor boards; and

realigning the local timer a processor board with time information contained in a received timing cell when its local timer drifts from the received time information outside of a predetermined time window.

17. The method of claim 16, wherein the predetermined time window is approximately 2 ms.

18. The method of claim 16, further comprising transmitting the timing cells to the processor boards over an Asynchronous Transfer Mode (ATM) network.

19. The method of claim 16, further comprising transmitting the timing cells to the processor boards over an Ethernet network.

20. The method of claim 16, further comprising transmitting the timing cells to the processor boards over a Universal Serial Bus.

21. The method of claim 16, wherein generating the timing cells comprises

receiving a universal coordinated time from a GPS receiver;

receiving a references clock from a PSTN; and

basing the time information contained in the timing cells on the received universal coordinated time and the received reference clock.

22. The method of claim 21, wherein the reference clock has a frequency of 8 KHz.